

DISCIPLINE SPECIFIC ELECTIVE COURSE – PHYSICS DSE 14: VERILOG AND FPGA BASED SYSTEM DESIGN

Course Title & Code	Credits	Credit distribution of the course			Eligibility Criteria	Pre-requisite of the course
		Lecture	Tutorial	Practical		
Verilog and FPGA based System Design Physics DSE 14	4	2	0	2	Class XII pass with Physics and Mathematics as main subjects	Basics of digital electronics

LEARNING OBJECTIVES

This course trains the students to use VLSI design methodologies and simulate simple digital systems. Students will understand the HDL design flow and the fundamental Verilog concepts in-lieu of today's most advanced digital design techniques. The emphasis of this course is to enhance the understanding of Programmable Logic Devices so as to implement the Digital Designs on FPGAs using Verilog HDL

LEARNING OUTCOMES

At the end of this course, students will be able to,

- Write synthesizable Verilog code.
- Write a Verilog test bench to test Digital Logic Design.
- Design and simulate digital circuits using Verilog modules.
- Understand various types of programmable logic building blocks such as PAL, PLA, CPLDs and FPGAs and their trade-offs.
- Design and implement digital systems on programmable logic device FPGA using Verilog HDL.

SYLLABUS OF PHYSICS DSE 14

THEORY COMPONENT

Unit – I

(20 Hours)

Introduction to Verilog: Introduction to HDL, importance of HDL, popularity of Verilog HDL, design flow, structure of HDL module, Verilog modules (design and stimulus), introduction to language elements - keywords, identifiers, white space, comments, format, integers, real and strings, logic values, data types, scalars and vector nets, parameters, system tasks, compiler directives

Gate level modelling: Introduction, built in primitive gates, buffers, multiple input gates, gate delays.

Data flow modelling: Continuous assignment, net declaration assignments, net delays, operator types and operators precedence

Behavioral modelling: Always and initial constructs, procedural assignment (blocking and non-blocking statements), If-else, case statements, loop structures (while, for, repeat and forever), sequential and parallel Blocks

Modelling of combinational and sequential digital circuits using different levels of abstraction

Hierarchical modelling concepts: Design methodologies, design a 4-bit adder using four 1-bit full adders

Unit – II **(10 Hours)**

Look up Tables: 2-input, 3-input and 4-input LUTs, Implement logic functions with LUT, advantages and disadvantages of lookup tables

Programmable Logic Devices: Difference between PAL and PLA, Realize simple logic functions using PAL and PLA, CPLD and FPGA architectures, types of FPGA, logic cell structure, programmable interconnects, logic blocks and I/O Ports, placement and routing, applications of FPGAs

References:

Essential Readings:

- 1) Verilog HDL. Pearson Education, S. Palnitkar, 2nd edition, 2003
- 2) FPGA Based System Design. W. Wolf, Pearson Education
- 3) Digital Signal processing, S. K. Mitra, 1998, McGraw Hill
- 4) VLSI design, D. P. Das, 2nd edition, 2015, Oxford University Press.
- 5) Digital Signal Processing with FPGAs, U. Meyer Baese, Springer, 2004

Additional Readings:

- 1) Fundamentals of Digital Logic with Verilog Design, S. B. Zvonko Vranesic, 2016, McGraw Hill

PRACTICAL COMPONENT

(15 Weeks with 4 hours of laboratory session per week)

- Session on how to write the design module and test benches using required software and simulate the combinational and sequential circuits.
- Sessions on how to configure FPGA using Verilog HDL for the final implementation of the logic design.

At least six experiments to be performed from the following list

- 1) Half adder, Full Adder using basic and derived gates.
- 2) Half subtractor and Full Subtractor using basic and derived gates.
- 3) Design and simulate 4-bit Adder using Data Flow Modeling.
- 4) Multiplexer (4x1) and Demultiplexer(1X4) using Data Flow Modeling.
- 5) Decoder and Encoder using case structure/gates.
- 6) Clocked D, JK and T Flip flops (with Reset inputs)
- 7) 4-bit Synchronous up/downCounter
- 8) To design and study switching circuits (LED blink shift)
- 9) To interface LCD using FPGA
- 10) To interface a multiplexed seven segment display.
- 11) To interface a stepper motor and DC motor.

References for laboratory work:

- 1) Digital System Designs and Practices: Using Verilog HDL and FPGAs, Ming-Bo Lin, Wiley India Pvt Ltd.

- 2) Verilog Digital System Design, Z. Navabi, 2nd edition, TMH
- 3) Designing Digital Computer Systems with Verilog, D. J. Laja and S. Sapatnekar, 2015, Cambridge University Press
- 4) Verilog HDL primer, J. Bhasker. BSP, 2nd edition, 2003