DISCIPLINE SPECIFIC ELECTIVE COURSE – 2: VHDL Programming(INDSE3B)

CREDIT DISTRIBUTION, ELIGIBILITY AND PRE-REQUISITES OF THE COURSE

Course title & Code	Credits	Credit distribution of the course			Eligibility criteria	Pre-requisite of the course (if any)
		Lecture	Tutorial	Practical/ Practice		
VHDL Programming (INDSE3B)	04	02	0	02	Course admission eligibility	Understanding of Digital Electronics

Learning Objectives

The Learning Objectives of this course are as follows:

- To develop the basic understanding of VHDL Modules, entity and architectures.
- To familiarize with different VHDL elements, Keywords and Identifiers
- To describe hardware in VHDL using different Modeling styles.
- To understand concurrent and sequential assignments.
- To introduce built in primitive gates and understand Gate level Modelling

Learning outcomes

The Learning Outcomes of this course are as follows:

- Learn about HDL Modules and simulation tools.
- Apply the knowledge of entity, architectures, VHDL Modules to describe hardware.
- Write and analyze various VHDL codes for combinational and sequential logic circuits
- describe hardware using multiple modeling styles.

SYLLABUS OF DSE-2

UNIT – I **(8 hours)**

Introduction to VHDL: A Brief History of HDL, Structure of HDL Module, Comparison of VHDL and Verilog, Introduction to Simulation and Synthesis Tools, VHDL requirements, VHDL basic language elements, Keywords, Identifiers, White Space Characters, Comments, format, VHDL operators.

VHDL Modeling: Describing hardware in VHDL, entity, architectures, VHDL Modules, Delays, data flow style, behavioural style, structural style, mixed design style, simulating design.

UNIT – II **(8 hours)**

BehavioralModeling: Introduction to behavioural modelling, Signal assignment,

Concurrent and sequential assignments., Entity Declaration, Architecture Body, BehavioralModeling, Process statement, Loop control statements, Multiple Processes, Delay Models, inertial delay model, transport delay model, transport vs inertial delay, Signal Drivers.

UNIT – III **(7 hours)**

Dataflow and Structural Modeling: Data flow Modeling, Concurrent Assignment statements, Block statements, Structural Modeling, Component declaration and Instantiation, generate statements, Process, IF, CASE, LOOP, NEXT, EXIT and ASSERT statements.

UNIT – IV **(7 hours)**

Gate level modeling: Introduction, built in Primitive Gates, multiple input gates, Tri-state gates, pull gates, MOS switches, bidirectional switches, gate delay, array instances, implicit nets, Illustrative Examples (both combinational and sequential logic circuits).

Practical component: **(60 hours)**

Learning Scilab/MATLAB (Experiments based on available systems).
Exploration of Signals and Systems using Scilab/MATLAB.

1. Write code to realize basic and derived logic gates.
2. Half adder, Full Adder using basic and derived gates.
3. Half subtractor and Full Subtractor using basic and derived gates.
4. Clocked D FF, T FF and JK FF (with Reset inputs).
5. Multiplexer (4x1, 8x1) and Demultiplexer using logic gates.
6. Decoder (2x4, 3x8), Encoders and Priority Encoders.
7. Design and simulation of a 4-bit Adder.
8. Code converters (Binary to Gray and vice versa).
9. 3-bit Ripple counter.

Essential/recommended readings

1. J. Bhasker, VHDL Primer, Pearson, 3rd edition ,2015.
2. Volnei. A.Pedroni, Circuit Design with VHDL, MIT Press; Third edition, 2020
3. Sudhakar Yalamanchili, Introductory VHDL-From Simulation to Synthesis, Pearson Education India. First Edition, 2000

Suggestive readings

1. Douglas Perry, VHDL, McGraw-Hill Education; 4th edition, 2002
2. Charles.H.Roth, Digital system Design using VHDL, Cengage; 2nd edition, 2012

Note: Examination scheme and mode shall be as prescribed by the Examination Branch, University of Delhi, from time to time.